查询MC14553BCP供应商

MC14553B

3-Digit BCD Counter

The MC14553B 3–digit BCD counter consists of 3 negative edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on–chip oscillator provides the low–frequency scanning clock which drives the multiplexer output selector.

This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- TTL Compatible Outputs
- On–Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	–0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Pin	±10	mA
I_{out}	Output Current (DC or Transient) per Pin	+20	mA
P_D	Power Dissipation, per Package (Note 2.)	500	mW
T_A	Ambient Temperature Range	–55 to +125	°C
T_{stg}	Storage Temperature Range	–65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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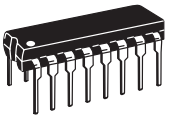
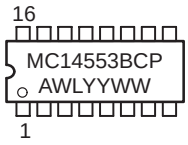
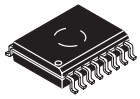
MARKING DIAGRAMS



PDIP–16
P SUFFIX
CASE 648





SOIC–16
DW SUFFIX
CASE 751G

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14553BCP	PDIP–16	25/Rail
MC14553BDW	SOIC–16	47/Rail

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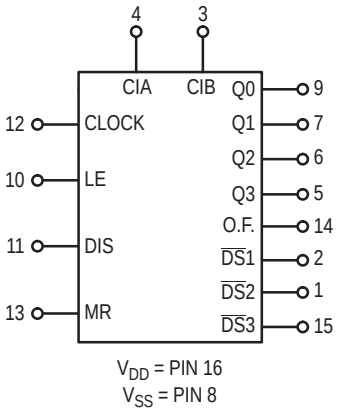
BLOCK DIAGRAM



TRUTH TABLE

Inputs				
Master Reset	Clock	Disable	LE	Outputs
0	↗	0	0	No Change
0	↘	0	0	Advance
0	X	1	X	No Change
0	1	↗	0	Advance
0	1	↘	0	No Change
0	0	X	X	No Change
0	X	X	↗	Latched
0	X	X	1	Latched
1	X	X	0	Q0 = Q1 = Q2 = Q3 = 0

X = Don’t Care

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (3.)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level V_{in} = V_{DD} or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
“1” Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 4.6 Vdc) Source —		5.0	– 0.25	—	– 0.2	– 0.36	—	0.14	—	
(V_{OH} = 9.5 Vdc) Pin 3		10	– 0.62	—	– 0.5	– 0.9	—	0.35	—	
(V_{OH} = 13.5 Vdc)		15	– 1.8	—	– 1.5	– 3.5	—	1.1	—	
(V_{OH} = 4.6 Vdc) Source —		5.0	– 0.64	—	– 0.51	– 0.88	—	– 0.36	—	mAdc
(V_{OH} = 9.5 Vdc) Other		10	– 1.6	—	– 1.3	– 2.25	—	– 0.9	—	
(V_{OH} = 13.5 Vdc) Outputs		15	– 4.2	—	– 3.4	– 8.8	—	– 2.4	—	
(V_{OL} = 0.4 Vdc) Sink —	I_{OL}	5.0	0.5	—	0.4	0.88	—	0.28	—	mAdc
(V_{OL} = 0.5 Vdc) Pin 3		10	1.1	—	0.9	2.25	—	0.65	—	
(V_{OL} = 1.5 Vdc)		15	1.8	—	1.5	8.8	—	1.20	—	
(V_{OL} = 0.4 Vdc) Sink — Other		5.0	3.0	—	2.5	4.0	—	1.6	—	mAdc
(V_{OL} = 0.5 Vdc) Outputs		10	6.0	—	5.0	8.0	—	3.5	—	
(V_{OL} = 1.5 Vdc)		15	18	—	15	20	—	10	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) MR = V_{DD}	I_{DD}	5.0	—	5.0	—	0.010	5.0	—	150	μAdc
		10	—	10	—	0.020	10	—	300	
		15	—	20	—	0.030	20	—	600	
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.35 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (0.85 μA/kHz) f + I_{DD}							
		15	I_T = (1.50 μA/kHz) f + I_{DD}							

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.004.

SWITCHING CHARACTERISTICS [6.] (C_L = 50 pF, T_A = 25°C)

Characteristic	Figure	Symbol	V_{DD}	Min	Typ [7.]	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	2a	t_{TLH}, t_{THL}	 5.0 10 15	 — — —	 100 50 40	 200 100 80	ns
Clock to BCD Out	2a	t_{PLH}, t_{PHL}	5.0 10 15	— — —	900 500 200	1800 1000 400	ns
Clock to Overflow	2a	t_{PHL}	5.0 10 15	— — —	600 400 200	1200 800 400	ns
Reset to BCD Out	2b	t_{PHL}	5.0 10 15	— — —	900 500 300	1800 1000 600	ns
Clock to Latch Enable Setup Time Master Reset to Latch Enable Setup Time	2b	t_{su}	5.0 10 15	600 400 200	300 200 100	— — —	ns
Removal Time Latch Enable to Clock	2b	t_{rem}	5.0 10 15	– 80 – 10 0	– 200 – 70 – 50	— — —	ns
Clock Pulse Width	2a	$t_{WH(cl)}$	5.0 10 15	550 200 150	275 100 75	— — —	ns
Reset Pulse Width	2b	$t_{WH(R)}$	5.0 10 15	1200 600 450	600 300 225	— — —	ns
Reset Removal Time	—	t_{rem}	5.0 10 15	– 80 0 20	– 180 – 50 – 30	— — —	ns
Input Clock Frequency	2a	f_{cl}	5.0 10 15	— — —	1.5 5.0 7.0	0.9 2.5 3.5	MHz
Input Clock Rise Time	2b	t_{TLH}	5.0 10 15	No Limit			ns
Disable, MR, Latch Enable Rise and Fall Times	—	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	15 5.0 4.0	µs
Scan Oscillator Frequency (C1 measured in µF)	1	f_{osc}	5.0 10 15	— — —	1.5/C1 4.2/C1 7.0/C1	— — —	Hz

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

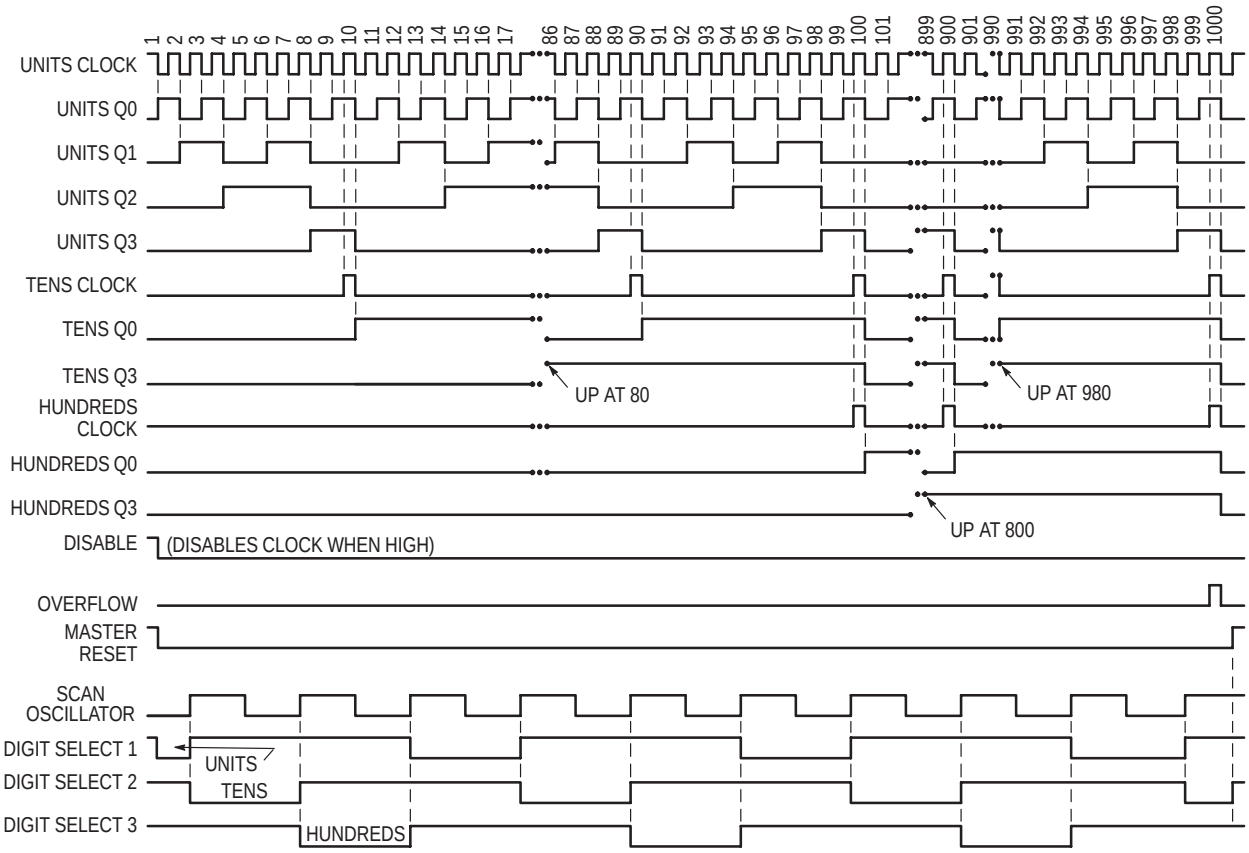


Figure 1. 3–Digit Counter Timing Diagram (Reference Figure 3)

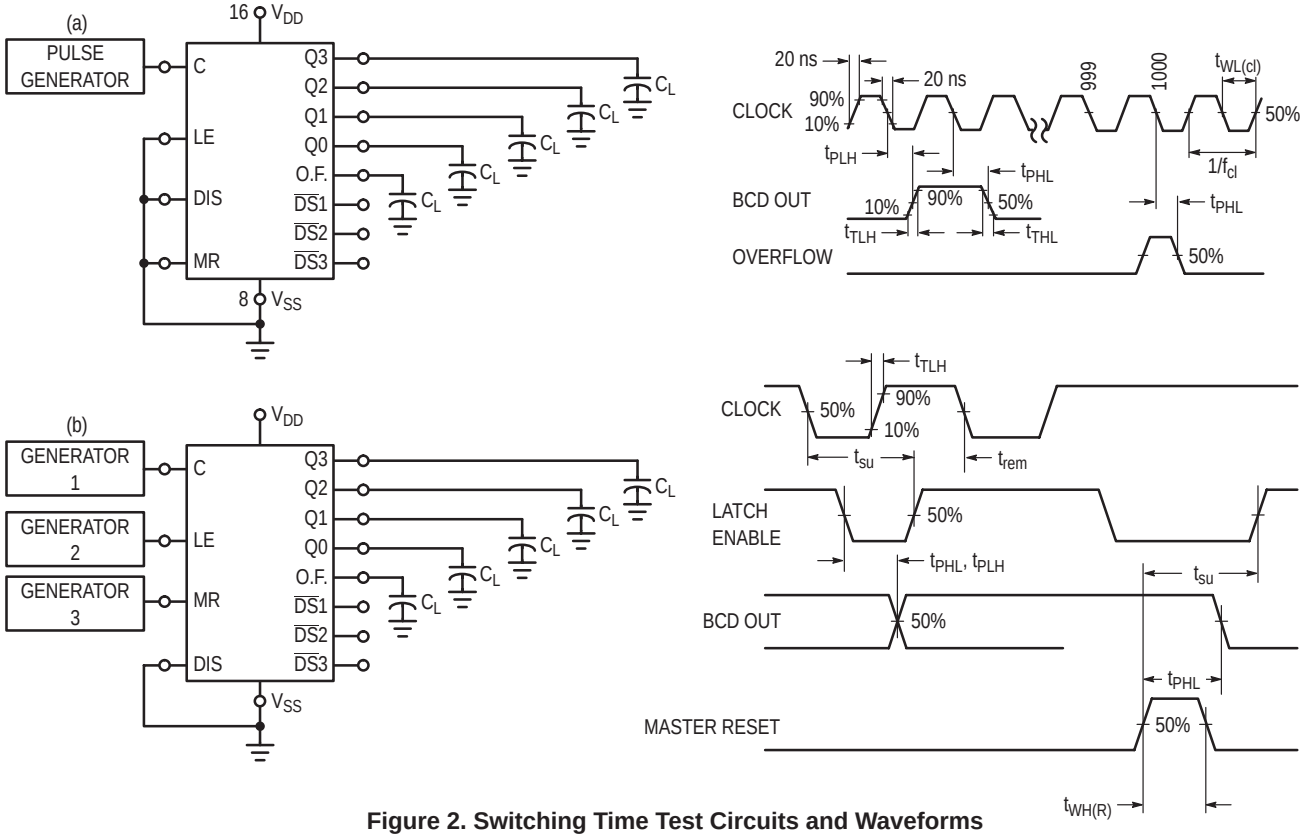


Figure 2. Switching Time Test Circuits and Waveforms

OPERATING CHARACTERISTICS

The MC14553B three–digit counter, shown in Figure 3, consists of three negative edge–triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active high), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active low) are provided for display control. All outputs are TTL compatible.

An on–chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4, or it can be overridden and driven with an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

The Master Reset input, when taken high, initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is high the digit scanner is set to digit one; but all three digit select outputs are disabled to prolong display life, and the scan oscillator is inhibited. The Disable input, when high, prevents the input clock from reaching the counters, while still retaining the last count. A pulse shaping circuit at the clock input permits the counters to continue operating on input pulses with very slow rise times. Information present in the counters when the latch input goes high, will be stored in the latches and will be retained while the latch input is high, independent of other inputs. Information can be recovered from the latches after the counters have been reset if Latch Enable remains high during the entire reset cycle.

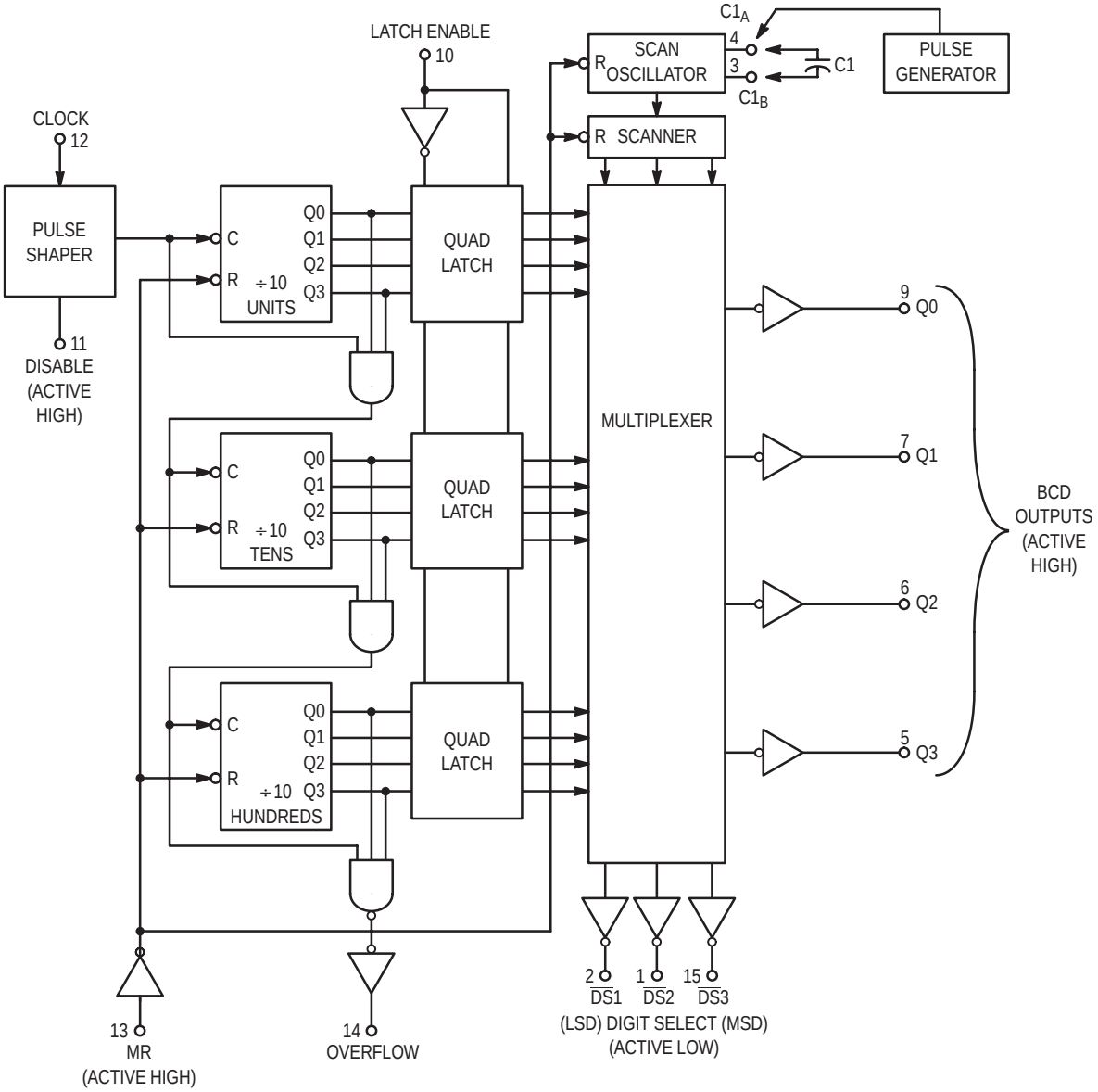


Figure 3. Expanded Block Diagram

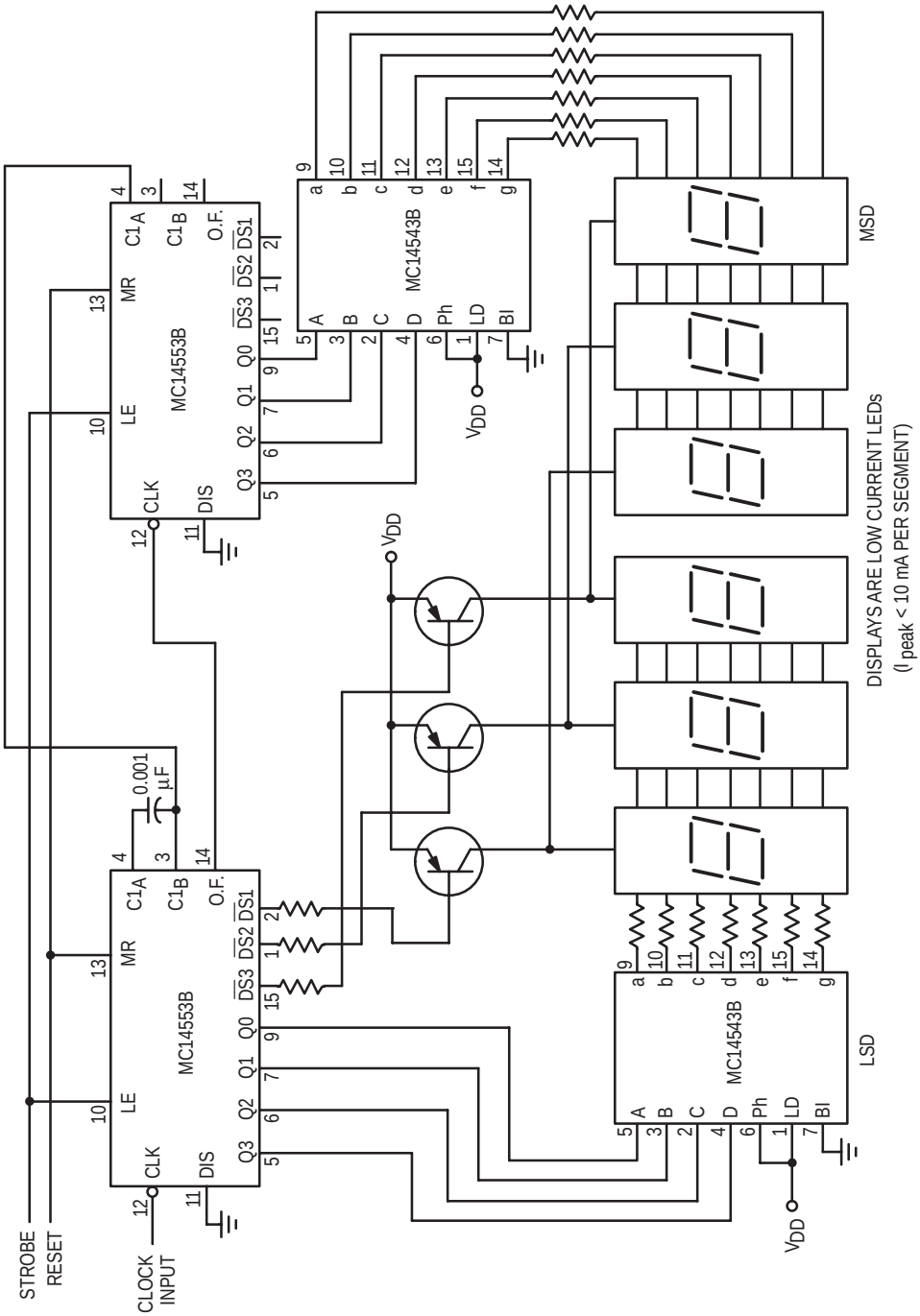
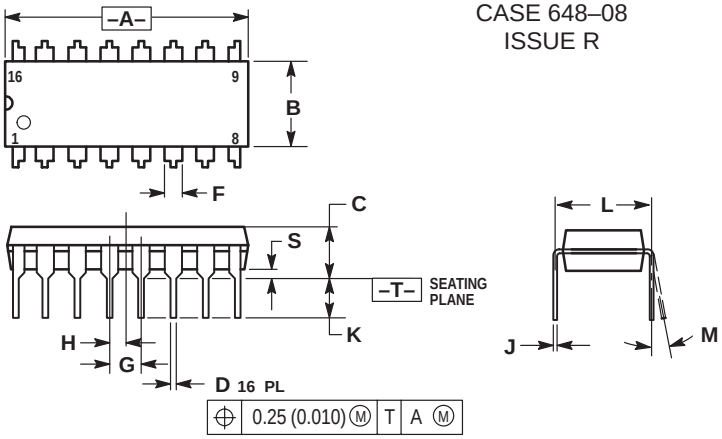


Figure 4. Six–Digit Display

PACKAGE DIMENSIONS

PDIP–16
P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

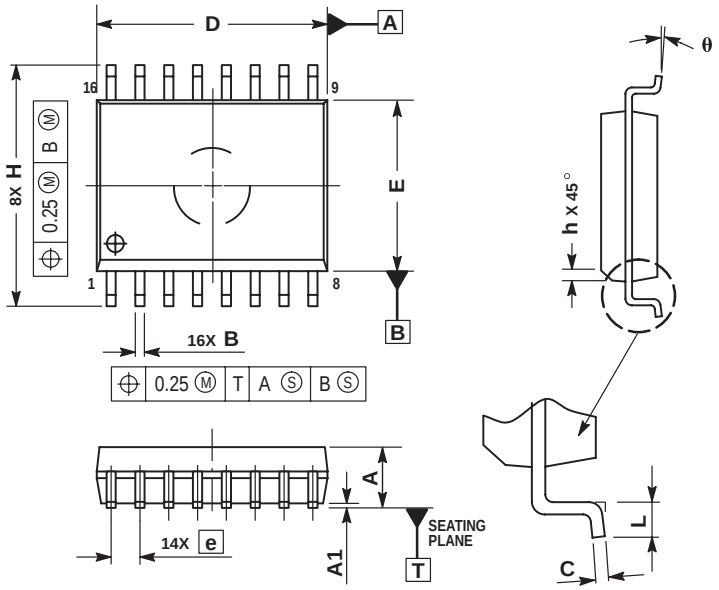


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

SOIC–16
DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–03
ISSUE B



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

Notes

Notes

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